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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,354	02/25/2004	Kie Y. Ahn	303.686US3	4551

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EXAMINER	
HUYNH, ANDY	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/786,354	AHN ET AL.	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *12-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-11* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/25/04,09/27/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

In the Response to the Restriction Requirement dated September 27, 2004, Applicant has elected without traverse, Species I, claims **1-11** is acknowledged. Accordingly, claims **12-17** are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 35 § 1.142(b) and MPEP § 821.03. Applicant has the right to file a divisional application covering the subject matter of the non-elected claims **12-17**.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed 02/25/2004 and 09/27/2004. The references cited on the PTOL 1449 form have been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims **1, 5-7, 9, and 10** are rejected under 35 U.S.C. 102(e) as being anticipated by Zhao (U.S. Patent No. 6,211,561), Applicant's submitted prior art (ASPA).

Regarding claim **1**, Zhao discloses in Figs. 1A-1B and the corresponding texts as set forth in column 4, lines 20-62, a multilevel wiring interconnect/a interconnect structure (10) in an integrated circuit, comprises:

a number of multilayer metal lines/conductive layers (16A-16D, 30, 32) connecting to a number of silicon devices in a substrate/a layer (12) (Layer (12) can be a semiconductor substrate formed from a semiconductor material, such as silicon. When layer (12) is a substrate, layer (12) can include transistors, diodes, and other semiconductor devices that are well known in the art) (col. 4, lines 22-27);

a low dielectric constant insulator/dielectric (18) in a number of interstices between the number of multilayer metal lines and the substrate/the layer; and

wherein the low dielectric constant insulator/dielectric includes a number of air gaps (22) in the low dielectric constant material.

Regarding claim **5**, Zhao discloses the number of multilayer metal lines including a number of multilayer metal lines/the conductive layers selected from the group consisting of Aluminum, Copper, Silver, and Gold (col. 8, lines 47-51).

Regarding claim **6**, Zhao discloses in Figs. 1A-1B the number of multilayer metal lines/the conductive layers includes a first conductor bridge level/a conductive plug (30) (col. 4, line 60).

Regarding claims **7, 9 and 10**, Zhao discloses in Figs. 1A-1B and the corresponding texts as set forth in column 4, lines 20-62, a multilevel wiring interconnect system/a interconnect structure (10), comprises:

a number of multilayer metal lines/conductive layers (16A-16D, 30, 32) connecting to a number of integrated circuit devices in a substrate/a layer (12) (Layer (12) can be a semiconductor substrate formed from a semiconductor material, such as silicon. When layer (12) is a substrate, layer (12) can include transistors, diodes, and other semiconductor devices that are well known in the art) (col. 4, lines 22-27); and

a low dielectric constant insulator/dielectric (18) in a number of interstices between the number of multilayer metal lines/the conductive layers and the substrate/the layer, the low dielectric constant insulator/dielectric having a number of air gaps (22) therein.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim **2** is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao (U.S. Patent No. 6,211,561), Applicant's submitted prior art (ASPA), in view of Jin et al. (USP: 6,059,553 hereinafter referred to as "Jin").

Zhao discloses the claimed limitations except for the multilevel wiring interconnect wherein the low dielectric constant insulator includes a low dielectric constant organic silica film. Jin teaches in Fig. 1 that an integrated circuit with an intermetal level dielectric (IMD) includes an organic-silica hybrid (110) and locates between metal lines (104) as set forth in the

Abstract. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the low dielectric constant insulator including a low dielectric constant organic silica film, as taught by Jin, in order to have lower permittivity for a given xerogel density and to increase material flexibility to limit brittleness problems during integrated circuit fabrication (col. 2, lines 22-25).

Claim **3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao (U.S. Patent No. 6,211,561), (ASPA), in view of Nag (USP: 6,214,719), (ASPA).

Zhao discloses the claimed invention except for the low dielectric constant insulator includes a low dielectric constant insulator having a dielectric constant (k) of less than 2.7. Nag teaches that the dielectric of the gap-fill region between the interconnect metal lines has dielectric constant to be on the order of k=1.9 to 2.5. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the low dielectric constant insulator having a dielectric constant of less than 2.7, as taught by Nag in order to reduce the RC signal delay and interline capacitance between interconnect metal lines (Nag, col. 5, lines 25-26).

Claim **8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao (U.S. Patent No. 6,211,561), (ASPA), in view of Bedner et al. (USP: 6,194,233 hereinafter referred to as "Bedner").

Zhao discloses the claimed limitations except for the number of multilayer metal lines are adapted to connect to at least one of a processor and a memory. Bedner teaches that in the ASIC environment for manufacturing custom logic circuits, components such as processors, memory arrays, and input and output interface circuits are integrated in a custom circuit and interconnected by metal wiring layers (col. 1, lines 14-18). It would have been obvious to one of

ordinary skill in the art at the time of the invention was made to connect and to adapt a process and a memory in a custom circuit and interconnected by metal wiring layers for system integration, as taught by Bedner.

Claim **11** is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao (U.S. Patent No. 6,211,561), (ASPA).

Zhao discloses the number of multilayer metal lines including a number of multilayer metal lines/the conductive layers selected from the group consisting of Aluminum, Copper, Silver, and Gold (col. 8, lines 47-51). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the number of multilayer metal lines consisting essentially of copper since it was known in the art that copper is preferred material for conductive materials because copper is relatively inexpensive, can be etched easily, and is a good conductor, both thermally and electrically.

Allowable Subject Matter

Claim **4** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Zhao, Jin, Bedner and Nag, taken alone or in combination, fail to teach the claimed limitation the multilevel wiring interconnect wherein the low dielectric constant insulator includes a film in which of a set methyl groups and a fluorine group of atoms are as much as 43% and 9% respectively of that for a content of silicon atoms in the film.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ah

10/08/04

Andy Huynh

Patent Examiner